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TRANSMITTAL FORM

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First Named Inventor	Tae Heon Lee
Art Unit	2814
Examiner Name	Cao, Phat X.
Attorney Docket Number	AMKOR-053G

ENCLOSURES *(Check all that apply)*

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  - ☐ Affidavits/declaration(s)
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RE: U.S. Patent Application No.: 10/763,859

Dear Sir/Madam:

Please correct the attached Filing Receipt which was mailed on January 27, 2003 as follows:

> **Domestic Priority as Claimed by Applicant:** The present application is a divisional of U.S. Application Serial No. 09/687,585 entitled SEMICONDUCTOR PACKAGE HAVING REDUCED THICKNESS filed October 13, 2000.

A copy of the originally filed marked-up specification indicating the domestic priority data is enclosed herewith for the purpose of reference only.

Should you have any questions regarding this application you may contact Applicant's representative at the number listed above.

Respectfully submitted,

Date: 9/14/05

By: _____

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EXHIBIT B: MARKED UP SUBSTITUTE SPECIFICATION

SEMICONDUCTOR PACKAGE HAVING REDUCED THICKNESS

INVENTORS

Tae Heon Lee
Mu Hwan Seo

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a divisional of U.S. Application Serial No. 09/687,585 entitled SEMICONDUCTOR PACKAGE HAVING REDUCED THICKNESS filed October 13, 2000.

STATEMENT RE: FEDERALLY SPONSORED RESEARCH/DEVELOPMENT

[0002] Not Applicable

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

[0003] The present invention relates to a semiconductor package and, more particularly, but not by way of limitation, to a semiconductor package that has a reduced thickness.

2. HISTORY OF RELATED ART

[0004] It is conventional in the electronic industry to encapsulate one or more semiconductor devices, such as integrated circuit dies, or chips, in a semiconductor package. These plastic packages protect a chip from environmental hazards, and provide a method and apparatus for electrically and mechanically attaching the chip to an intended device. Recently, such semiconductor packages have included metal leadframes for supporting an integrated circuit chip which is bonded to a chip paddle region formed centrally therein. Bond wires which electrically connect pads on the integrated circuit chip to individual leads of the leadframe are then incorporated. A hard plastic encapsulating material, or encapsulant, which covers the bond wire, the integrated circuit chip and other components, forms the exterior of the package. A primary focus in this design is to provide the chip with adequate protection from the external environment in a reliable and effective manner.

[0005] As set forth above, the semiconductor package therein described incorporates a leadframe as the central supporting structure of such a package. A portion of the leadframe completely surrounded by the plastic encapsulant is internal to the package. Portions of the leadframe extend internally from the package and are then used to connect the package externally. More information relative to leadframe technology may be found in Chapter 8 of the book Micro Electronics Packaging Handbook, (1989), edited by R. Tummala and E. Rymaszewski. This book is published by Van Nostrand Reinhold, 115 Fifth Avenue, New York, New York, which is herein incorporated by reference.

[0006] Once the integrated circuit chips have been produced and encapsulated in semiconductor packages described above, they may be used in a wide variety of electronic appliances. The variety of electronic devices utilizing semiconductor packages has grown dramatically in recent years. These devices include cellular phones, portable computers, etc. Each of these devices typically include a motherboard on which a significant number of such semiconductor packages are secured to provide multiple electronic functions. These electronic appliances are typically manufactured in reduced sizes and at reduced costs, which has resulted in increased consumer demand. Accordingly, not only are semiconductor chips highly integrated, but also semiconductor packages are highly miniaturized with an increased level of package mounting density.

[0007] According to such miniaturization tendency, semiconductor packages, which transmit electrical signals from semiconductor chips to motherboards and support the semiconductor chips on the motherboards, have been designed to have a size of about 1x1mm. ~~Examples of such semiconductor packages are referred to as MLF (micro leadframe) type semiconductor packages and MLP (micro leadframe package) type semiconductor packages. Both MLF type semiconductor packages and MLP type semiconductor packages are generally manufactured in the same manner.~~

[0008] One obstacle to reducing the thickness of conventional semiconductor packages is the internal leads are as thick as the chip paddle. Under the condition that the thickness of the internal leads is identical to that of the chip paddle, the bond pads on the semiconductor chip that is mounted onto the chip paddle are positioned at a far higher level than are the internal leads, so that the loop height of the conductive wires for connecting the semiconductor chip and the internal leads is elevated. The loop height results in an increase in a wire sweeping phenomenon

that is caused by pressure of an encapsulation material during encapsulation of the package components.

[0009] Previously, techniques for reducing the thickness of semiconductor packages have been utilized, such as back-grinding techniques in which a semiconductor chip is ground down before being mounted on a chip paddle. The back-grinding process, however, deleteriously affects the semiconductor chip. For example, a semiconductor chip that is thinned in this manner is apt to undergo ~~warpage~~ **warping,** which may result in damaging the internal integrated circuits. In addition, the semiconductor chip itself may be cracked during the back-grinding.

BRIEF SUMMARY OF THE INVENTION

[0010] The **various embodiments of the** present invention ~~provides~~ **provide** a semiconductor package that is extremely thin without the need for conducting a back-grinding process or at least for reducing the amount of back-grinding that is required. In one embodiment of the present invention, there is provided a semiconductor package comprising a semiconductor chip provided with a plurality of bond pads, a chip paddle bonded to the bottom surface of the semiconductor chip via an adhesive, a plurality of ~~internal~~ leads formed at regular intervals along the ~~circumference~~ **perimeter** of the chip paddle and conductive wires for electrically connecting the bond pads of the semiconductor chip to the ~~internal~~ leads. A package body comprises the semiconductor chip, the conductive wires, the chip paddle and the ~~internal~~ leads that are preferably encapsulated by an encapsulation material. The chip paddle, the ~~internal~~ leads and the tie bars are externally exposed at their side surfaces and bottom surfaces. The chip paddle is half-etched over the entire upper surface of the chip paddle, which results in a thinner thickness than the ~~internal~~ leads. In one ~~version~~ **embodiment** of the **present** invention, the half-etched chip paddle is about 25-75% as thick as the ~~internal~~ leads. Accordingly, by half-etching the entire upper surface of the chip paddle, the chip paddle itself is made thinner than the ~~internal~~ leads, leading to the slimming of the semiconductor package.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] A more complete understanding of the method and apparatus of the present invention may be obtained by reference to the following detailed description, **with like reference numerals denoting like elements,** when taken in conjunction with the accompanying drawings wherein:

[0012] FIGURE 1 is a cutaway perspective view of a semiconductor package incorporating the improved leadframe assembly of the present invention.

[0013] FIGURE 2 shows a cross ~~sectional elevational view~~ **section** of a semiconductor package wherein the semiconductor package has a chip paddle of reduced thickness according to one embodiment of the present invention; and

[0014] FIGURE 3 shows a bottom plan view of the semiconductor package of Figure 1.

~~DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS~~

[0015] The present invention may be understood more readily by reference to the following detailed description of preferred embodiments of the **present** invention and the figures.

DETAILED DESCRIPTION OF THE INVENTION

[0016] Referring now to Figures 1, 2 and 3, a representative ~~MLF type~~ semiconductor package embodying aspects of the present invention is designated generally 10. Semiconductor package 10 comprises a semiconductor chip 12. Semiconductor ~~chip12~~ **chip 12** has a plurality of bond pads 14 on an upper surface of semiconductor chip 12 and along ~~a circumference~~ **the perimeter** of semiconductor chip 12. A chip paddle 16 is bonded to a bottom surface of semiconductor chip 12 via an adhesive. At a corner of chip paddle 16 is a tie bar 20 (Figures 1 & 2), which extends outwards toward a respective corner of the ~~conductor~~ **semiconductor** package 10. The tie bar 20 preferably also has a half-etched portion 21 (Fig. 1).

[0017] A plurality of ~~internal~~ leads 22 are located along the circumference of chip paddle 16. The chip paddle 16 and the ~~internal~~ leads 22 are externally exposed at their bottom surfaces (see Figure 2). Additionally, the ~~internal~~ leads 22 are exposed on their side faces (see Figure 1). The externally exposed portions of the chip paddle 16 and the ~~internal~~ leads 22 may be electroplated with a corrosion minimizing material such as, but not limited to, tin lead, gold, nickel palladium, tin bismuth, or other similar materials known in the art. Each of ~~internal~~ leads 22 has a half-etched portion 24 at an end facing the chip paddle 16. The upper surface of each of ~~internal~~

leads 22 may also be electroplated with an electrical conductivity enhancing material such as, for example, gold or silver. Conductive wires 26 provide an electrical pathway between the bond pads 14 of the semiconductor chip 12 and the ~~internal~~ leads 22. The semiconductor chip 12, the conductive wires 26, the chip paddle 16 and the ~~internal~~ leads 22 are encapsulated by an encapsulation material 28 to create a package body 30 whereas the chip paddle 16, the ~~internal~~ leads 22 and the tie bars 20 are externally exposed toward the downward direction of the **semiconductor** package ~~body~~ 10. The encapsulation material 28 may be thermoplastics or thermoset resins, with the thermoset resins including silicones, phenolics, and epoxies.

[0018] An aspect **of the various embodiments** of the present invention resides in the formation of a half etched surface 32 over the entire upper surface of the chip paddle 16, so as to make the thickness of the chip paddle 16, designated h2 (Figure 2), smaller than **the thickness of** the ~~internal~~ lead 22, which is designated h1 (Figure 2). Preferably, the chip paddle 16 is about 25-75% as thick as the ~~internal~~ leads 22, but this range is presented for example only and should not be construed to limit the present invention.

[0019] It is also preferred that the formation of the half-etched surface 32 over the entire upper surface of the chip paddle 16 is conducted while a lower side area of the ~~internal~~ lead **22** is etched, e.g., to form half etched ~~position~~ **portion** 24. However, the present invention is not limited to etching the top surface of chip paddle 16 and the half etched ~~position~~ **portion** 24 of the ~~internal~~ leads 22 ~~may be formed~~ simultaneously.

[0020] By half-etching the entire upper surface of the chip paddle 16, the total height of the semiconductor package body 30 is reduced. When semiconductor chip 12 **is** mounted on the half-etched surface 32 of the chip paddle 16, the semiconductor chip 12 is positioned at a lower height than the semiconductor chip 12 would be if it were located on a non-etched chip paddle 16. Thus, the loop height of the conductive wires 26 is also lowered. An additional benefit is that the lower loop height of the conductive wires 26 decreases an occurrence of wire sweeping during encapsulation of the semiconductor package 10. Further, the low height of the semiconductor chip 12 results in decreasing the thickness of the **semiconductor** package ~~body~~ 10.

[0021] The present invention has been described in an illustrative manner, and it is to be understood the terminology used is intended to be in the nature of descriptions rather than of

limitation. Many modifications and variations of the present invention are possible in light of the above teachings.

[0022] As described hereinbefore, the chip paddle 16 is made thinner than the ~~internal~~ leads 22 by half-etching the entire upper surface of the chip paddle 16, so that the total thickness of the semiconductor package 10 can be decreased. In addition, the height of semiconductor chip 12 with respect to the bottom surface of chip paddle 16 is reduced when the semiconductor chip **12** is mounted on the half-etched chip paddle **16**. Consequently, the loop height of the conductive wires 26 is also lowered, which reduces wire sweeping during the encapsulation of the semiconductor package **10**.

[0023] The following applications are being filed on the same date as the present application and are all incorporated by reference as if wholly rewritten entirely herein, including any additional matter incorporated by reference therein:

~~Docket~~ **Patent/Serial** No.	Title of Application	First Named Inventor
~~45475-00013~~ **6,646,339**	Improved Thin and Heat Radiant Semiconductor Package and Method for Manufacturing	Jae Hun Ku
~~45475-00014~~ **6,627,976**	Leadframe for Semiconductor Package and Mold for Molding the Same	Young Suk Chung
~~45475-00017~~ **6,475,827**	Method for Making a Semiconductor Package Having Improved Defect Testing and Increased Production Yield	Tae Heon Lee
~~45475-00018~~ **6,639308**	Near Chip Size Semiconductor Package	Sean Timothy Crowley
~~45475-00022~~ **6,677,663**	End Grid Array Semiconductor Package	Jae Hun Ku
~~45475-00026~~ **09/687,048**	Leadframe and Semiconductor Package with Improved Solder Joint Strength	Tae Heon Lee
~~45475-00029~~ **6,555,899**	Semiconductor Leadframe Assembly and Method of Manufacture	Young Suk Chung
~~45475-00030~~	~~Improved Method for Making~~	Young Suk Chung

6,525,406	~~Semiconductor Packages~~ **Semiconductor Device Having Increased Moisture Path and Increased Solder Joint Strength**	

[0024] It is this believed that the operation and construction of the present invention will be apparent from the foregoing description of the preferred exemplary embodiments. It will be obvious to a person of ordinary skill in the art that various changes and modifications may be made herein without departing from the spirit and the scope of the invention.

SEMICONDUCTOR PACKAGE HAVING REDUCED THICKNESS

ABSTRACT **OF THE DISCLOSURE**

[0025] A semiconductor package is disclosed that comprises a chip paddle and a semiconductor chip that has a plurality of bond pads. The semiconductor chip is located on an upper surface of the chip paddle. ~~Internal leads~~ **Leads** are formed at intervals along ~~a circumference~~ **the perimeter** of the chip paddle. The ~~internal~~ leads are in electrical communication with the bond pads. The semiconductor chip, the chip paddle and the ~~internal~~ leads are encapsulating by an encapsulation material. The height of the semiconductor package of the invention is minimized by half etching the chip paddle to reduce the thickness of the chip paddle such that the thickness of the chip paddle such that the thickness of the chip paddle is less than the thickness of the ~~internal~~ leads. Preferably, the chip paddle of the **present** invention is about 25-75% of the thickness of the ~~internal~~ leads.

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Applicant(s)

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Domestic Priority data as claimed by applicant

Foreign Applications

REPUBLIC OF KOREA 99-44651 10/15/1999

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Early Publication Request: No

Title

Semiconductor package having reduced thickness

Preliminary Class

ATTORNEY DOCKET NO: AMKOR-053G
TITLE: SEMICONDUCTOR PACKAGE HAVING REDUCED THICKNESS

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